REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave Blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	June 13, 1997	Final Sept 96 - June 97

4. TITLE AND SUBTITLE

Low Energy/Low Noise Electronic Components for Mobile Platform Applications

5. FUNDING NUMBERS

DAAH04-96-C-0079

6. AUTHOR(S)

Mr. S. K. Leong
Prof. Krishna Shenai

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Polyfet RF Devices
1110 Avenida Acaso, Camarillo, CA 93012
University of Illinois at Chicago
809 South Marshfield Avenue, 511 MB
Chicago, IL 60612-7205

8. PERFORMING ORGANIZATION REPORT NUMBER

STTR01

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Department of the Army, Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

ARO 36082.1-EL-ST

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (*Maximum 200 words*)

We prototyped Polyfet RF Device's 80VLDMOSFETs on bulk silicon substrates using advanced numerical two-dimensional (2D-) finite-element semiconductor process and device simulators and showed excellent agreement between measured and simulated DC and RF parameters. This infrastructure was then used to develop a number of 40V LDMOSFET designs, both on bulk silicon and SOI material, and identify optimum device structures suitable for further development in Phase II. Our Phase I research has shown the SOI LDMOSFETs promise significant improvements in gain, noise figure, efficiency and manufacturing cost compared to bulk devices. These results are highly promising and provide the impetus for further investigation and development.

14. SUBJECT TERMS

STTR Report, SOI, RF, Mobile, Amplifier

15. NUMBER OF PAGES

31

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

Final Report

STTR Contract DAAH04-C-0079

Low Energy / Low Noise Elec. Comp. for Mobile Platform Apps.

Army 96T007

by

Polyfet RF Devices

Friday, June 13, 1997

Table of Contents

Abstract

We prototyped Polyfet RF Device's 80V LDMOSFETs on bulk silicon substrates using advanced numerical two-dimensional (2D-) finite-element semiconductor process and device simulators and showed excellent agreement between measured and simulated DC and RF parameters. This infrastructure was then used to develop a number of 40V LDMOSFET designs, both on bulk silicon and SOI material, and identify optimum device structures suitable for further development in Phase II. Our Phase I research has shown that SOI LDMOSFETs promise significant improvements in gain, noise figure, efficiency, and manufacturing cost compared to bulk devices. These results are highly promising and provide the impetus for further investigation and development.

C. Phase I Activities

C1. Introduction

Next generation terrestrial and space technologies for civilian and military applications require broad band signal processing capability over frequencies that include upper MF, HF, VHF, UHF and L bands. Most applications are mobile, so prime power is severely limited. Size, weight, and cost are also critical. The generation, amplification, distribution and conditioning of on chip power become serious concerns, and in many cases, are important "show stoppers." It is the intent of this project to develop low-cost highly efficient integrated RF silicon-on insulator (SOI) power lateral double-diffused MOSFET (LDMOSFET) technologies for emerging wireless communication and portable computing applications.

The RF industry is currently actively pursuing the development of novel power MOSFET RF technologies for L-band (0.39 GHz - 1.55 GHz) applications. The RF performance of these new MOS technologies is at par with that of silicon bipolar transistors and GaAs MESFETs, opening up new exciting possibilities in RF and digital/analog integration with CMOS technologies [1,2]. In the power amplification areas, both vertical and lateral MOSFETs have been used for multi Watt amplifiers at frequencies below 1 GHz. As MOSFET technology is both simple and robust, which coupled with its excellent noise, power gain and linearity may make MOS devices major players in the portable communication market.

The circuit functions found in a portable radio include RF mixers, power amplifiers (PA), low-noise amplifiers (LNA) and voltage-controlled oscillators (VCO). The performance of state-of-the art [3-5] BJT and MOSFET components suggests that silicon MOSFETs are advantageous over BJTs for power amplification and points out that for LNAs and mixers, the MOSFET being a FET technology is more linear than BJTs. The VCO performance for MOSFETs is slightly inferior to that of BJTs, but still meets the specifications of cellular and various other radio applications.

The power amplifier industry is now moving towards custom-made transistors that are designed for optimum RF performance at the device level. This is required since the performance of the transistor, which is the fundamental element of the sub-system, determines the maximum achievable performance of the entire sub-system. These optimum devices are then integrated into the circuit boards and proper matching circuitry is built around them to obtain the maximum gain and linearity. Hence extensive understanding of the device physics is mandated during the design of the transistors for these applications. The RF performance of these devices is mainly affected by the parasitics inherent within the device[7,8]. These parasitics affect critical device performance parameters such as efficiency, gain and noise figure. An in-depth understanding of the device physics helps to predict the cause for these parasitics, and hence, find means for reducing these parasitics during device development. In this investigation, an advanced mixed device and circuit simulator was used to study the physical operating characteristics of the RF LDMOSFET at 1 GHz in which the transistor is represented as a two-dimensional (2D-) finite element grid structure. This approach allows for direct solution of semiconductor equations at various nodes in the mesh. Second order effects such as high-field transport and heat generation and diffusion are also included. This permits the study of the variation of depletion

region in the device with bias and other factors that control the parasitics within the device. The simulator also helps to study the high voltage behavior of the device, and hence, to optimize the design to prevent process dependent issues such as surface breakdown.

Silicon-on insulator (SOI) technology is now mature and is already being used to manufacture DRAMS, SRAMS, and even microprocessors [9]. A recent survey suggests that SOI technology offers the optimum speed times power product compared to even GaAs technology [10]. However, second order effects such as lattice heating need to be carefully taken into effect in order to develop optimum SOI devices. Our recent work has shown that self-heating can have deleterious effects in devices with feature dimensions below 1 micron [11]. Until recently, SOI CMOS technology has been driven and proven by the US Government for strategic-level radiation resistant DoD applications. As SOI material cost and quality have improved, commercial opportunities have become viable. High quality, low cost SOI CMOS material offers enormous payoff for commercial DRAMS and SRAMS, while also providing an optimal solution for natural space products. To take full advantage of SOI VLSI, we propose to develop 40V RF SOI power LDMOSFETs for next generation mobile communication and computing platforms.

C2. Prototyping of 80V Bulk Silicon LDMOSFET Device

Polyfet RF Devices has recently introduced [12] into the commercial market gold metallized 65V LDMOSFETs with an RF drain efficiency of 55%. Lateral devices are superior to vertical devices for RF applications since the source electrode can be contacted on the wafer back side, thus providing a viable common source configuration. The intent of this proposal is to further optimize these devices by employing new device designs and a low-cost SOI wafer fabrication technology. The new technology can then be applied beyond power amplifiers and in various RF functions found in portable communication and computing applications.

This section describes the methodology used for prototyping Polyfet's current 80V silicon RF LDMOSFET. The transistor was prototyped using the doping profiles extracted from an experimental device and extensive two dimensional (2D-) simulations were performed to characterize the DC and RF performance of the device. A good match between the measured and simulated data is reported. A simple circuit model was developed which accurately predicts the DC and RF characteristics in circuit simulators. It is shown through 2D- simulations that the LDD region in the LDMOSFET can be modeled as a JFET. A methodology for the accurate extraction of model parameters for the circuit model is discussed. It is shown that the DC and RF performances of the circuit model closely match the measured data. Advanced mixed device and circuit simulations were used to obtain S-parameters of the device which provide new insights into device physics and also the basis for statistical process control studies.

Optimum LDMOSFETs for lower voltage applications have been reported in the past [5-7]. Wood et al. [5] reported an LDMOSFET device operating with a 26V power supply providing a maximum gain of 11.2 dB and 44% drain efficiency. For determining the RF performance of the device, it is required that a circuit model be built which could emulate the RF performance of the device at specified bias conditions. There has been considerable work reported in the past on circuit models of these devices and also on the extraction of model parameters [8, 12-14]. The most desirable feature of the circuit model is its simplicity and ease with which model parameters can be extracted. The total number of components must be kept to a minimum to improve the simulation efficiency. The model

validity can be enhanced if its components can be associated with the physical principles of device operation. This feature is particularly relevant to semiconductor devices since in addition to predicting system performance, these models are used to estimate the sensitivity of a system to semiconductor processes and device parameter variations.

In this section, a systematic approach is used to prototype an LDMOSFET structure using the measured doping profiles obtained from the spreading resistance profiling (SRP) analysis and advanced 2D- process and device simulators. Extensive DC simulations were performed to study the static behavior of the device and the simulated results were compared with the measured data. A compact circuit model was developed by extracting the model parameters from the measured and simulated data. This model was used to perform DC and RF simulations. The circuit model was developed from an in-depth understanding of the physical operating principles of the device obtained from 2D- simulations. Mixed device and circuit simulations were also used to obtain S-parameters of the intrinsic device and the packaged device. A good match is obtained between the measured and modeled DC and RF performances. This validates the circuit model and also the method of extraction of the model parameters for the various components of this model. Detailed performance plots showing the comparison between the measured, simulated and modeled results are reported.

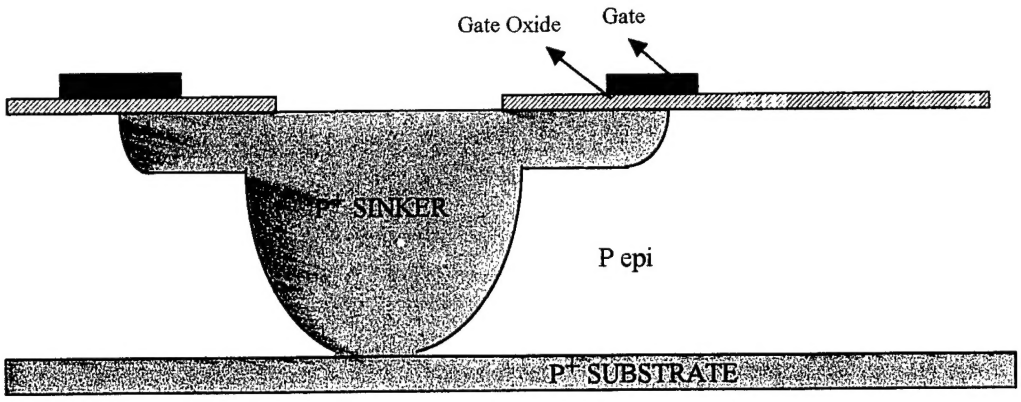
(i) Device Structure

A device structure for simulation was created using an advanced process simulator where the actual process recipe used for wafer fabrication served as the input. The device structure is represented as a 2D- finite element grid and the device simulator was then used to simulate the DC characteristics. Fig. 1(a) illustrates the cross section of the device following each critical process step. The basic device structure is shown in Fig.1(b) and corresponding feature dimensions for the device are listed Table 1. Minor changes were necessary in the doping profiles to obtain good agreement between the measured and simulated values of V_{BD} and V_{th}. Fig. 2 shows a typical comparison between the doping profile of the fabricated device (measured using the SRP analysis) and the simulated structure.

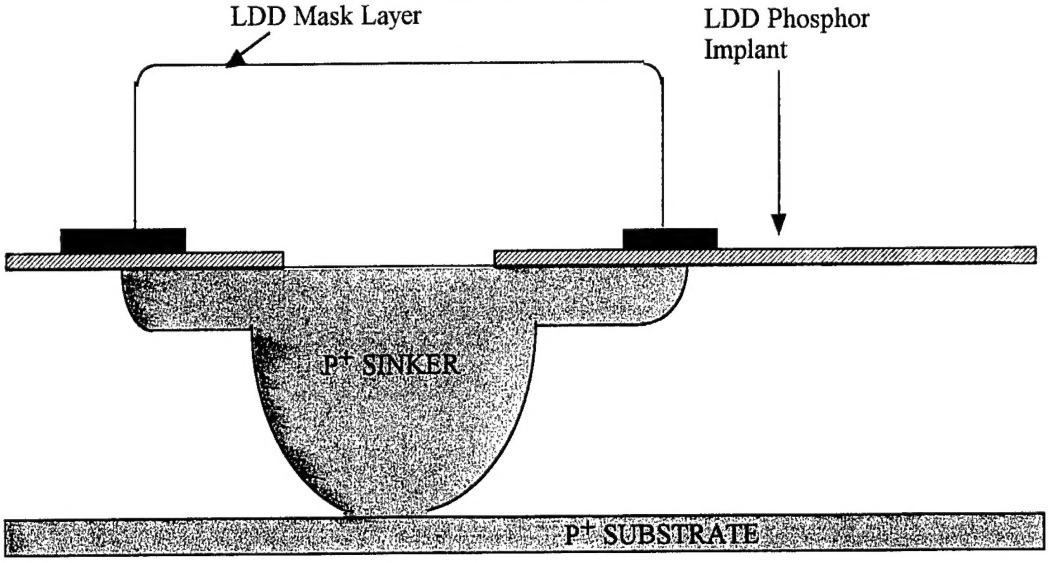
Table.1 Device feature dimensions

Parameter	Value (μm)
l_s	4.0
l_{so}	4.25
l_g	1.5
l_{ldd}	5.0
l_d	0.75

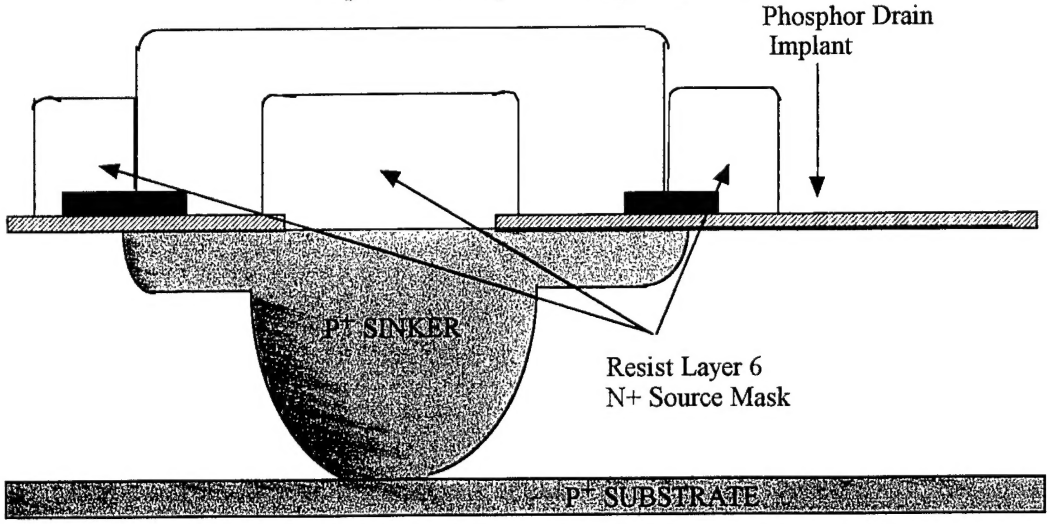
The device was fabricated on a 0.02 Ω-cm p-type substrate on which a 9 μm thick p-type epitaxial region (9 Ω-cm) was grown at 1000°C. A p-type sinker diffusion was used to ground the source to the substrate to minimize the common lead inductance and increase the RF gain. The p-type body region under the gate forms the channel. This device is operated with a power supply of 28 V, and hence, the device is required to be able to block at least two times the operating voltage that might be seen across the device due to inductive kickback. This is accomplished by the inclusion of the LDD region of the drain extension. In the absence of the LDD region, most of the applied drain voltage appears across



Step 1. Formation of Gate and Body

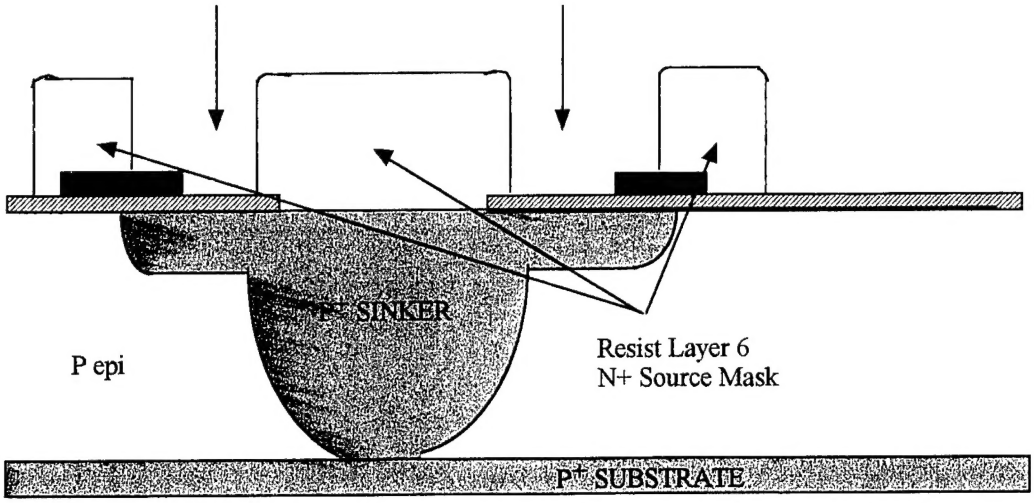


Step 2. LDD Implant through Layer 5.

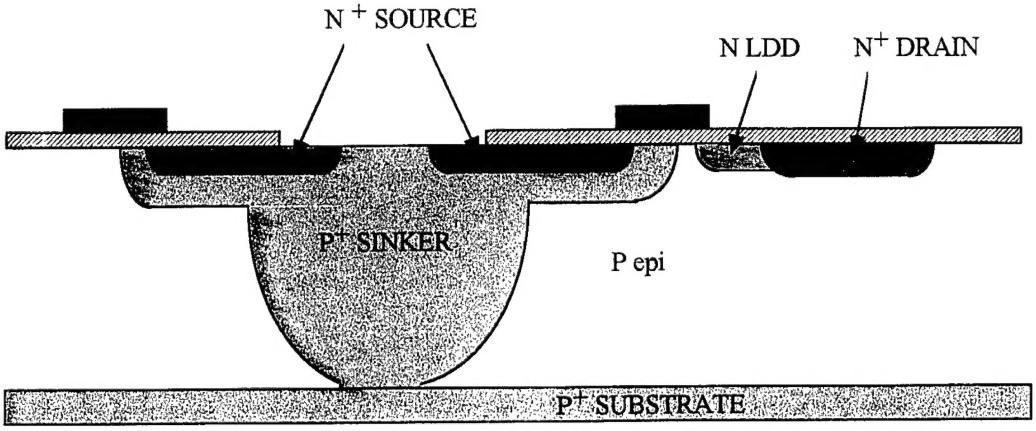


Step 3. Adding layer 6 to allow N^+ Drain Implant

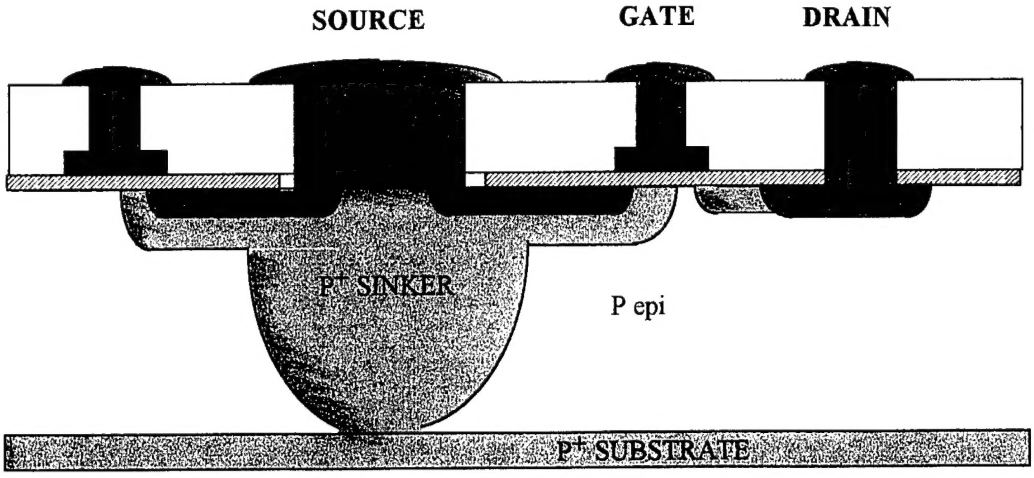
Fig. 1(a) Process sequence for 80V silicon RF LDMOSFET.



Step 4. Layer 6 by itself to do As Source Implant.



Step 5. Formation of N^+ Source, Drain and N LDD after 1000°C anneal.



Step 6. Final structure after metal mask.

Fig. 1(a) Process sequence for 80V silicon RF LDMOSFET (continued).

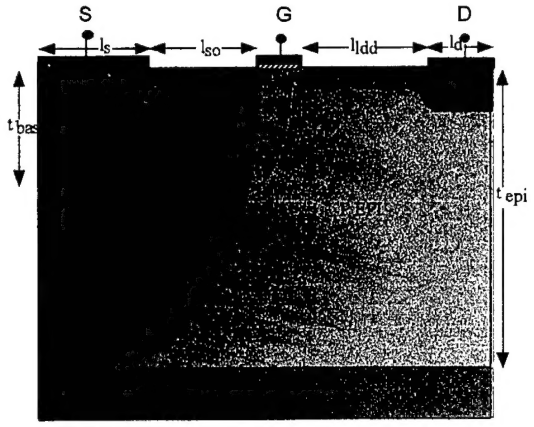


Fig. 1(b) Cross-section of LDMOSFET

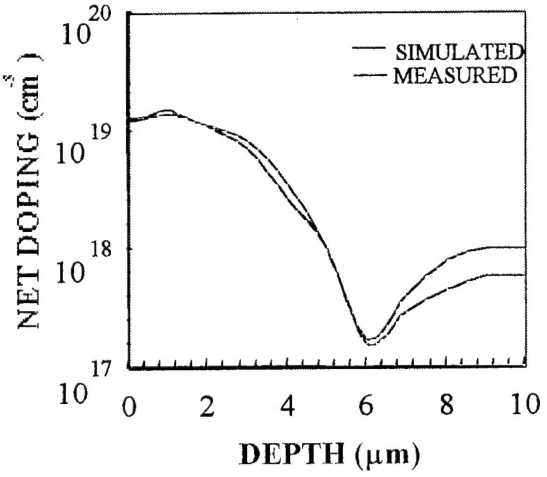


Fig.2 Doping profile under the gate

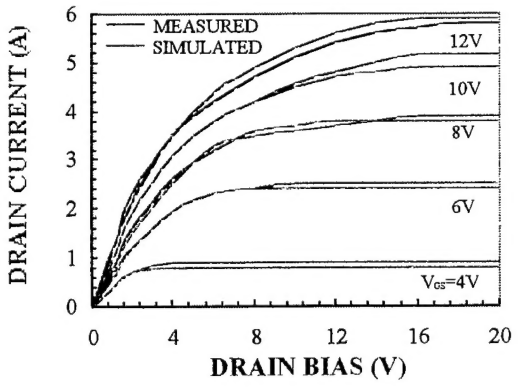


Fig.3 Simulated vs. Measured I_D-V_{DS} curves

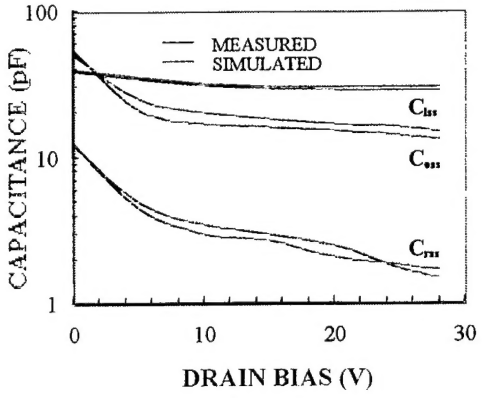


Fig.4 C-V Plots

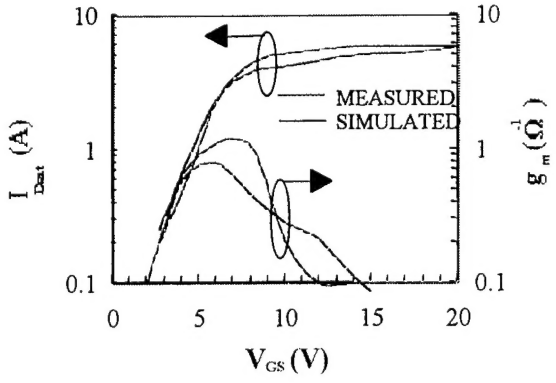


Fig. 5 Transconductance and I_{Dsat} vs. V_{GS}.

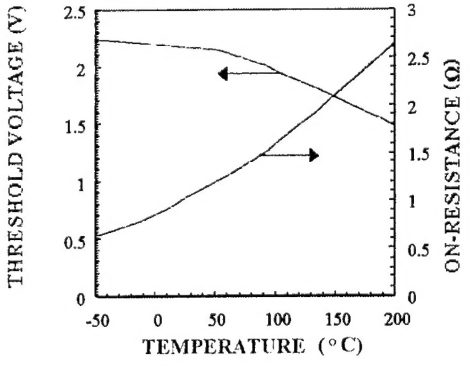


Fig.6 Variation of On-Resistance and V_{th} with temperature

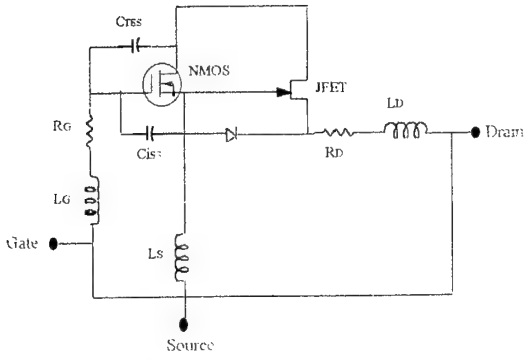


Fig. 7 Circuit model for LDMOSFET

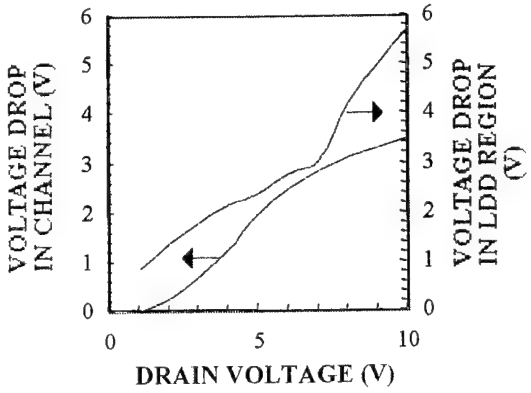


Fig.8 Plot showing voltage drop along channel and LDD

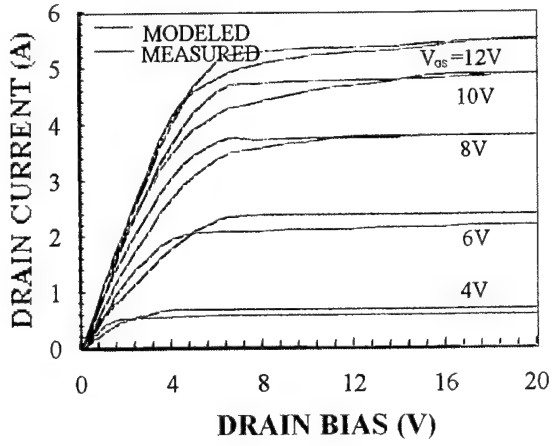


Fig.10(a) Measured and Modeled I-V curve

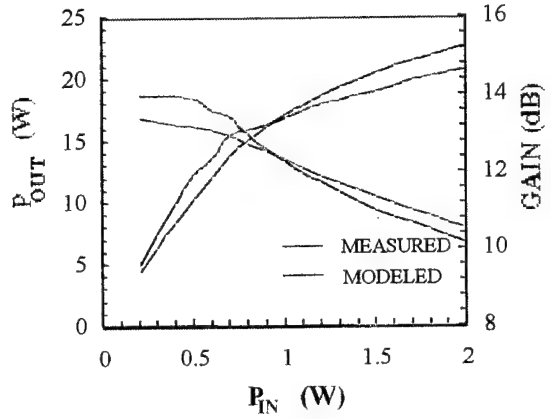
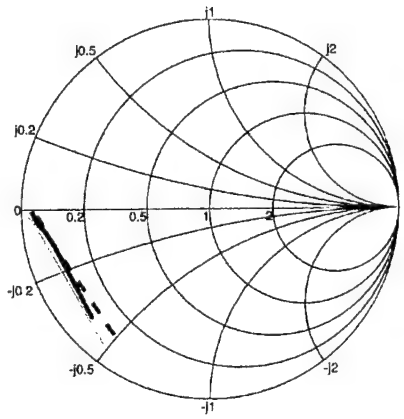
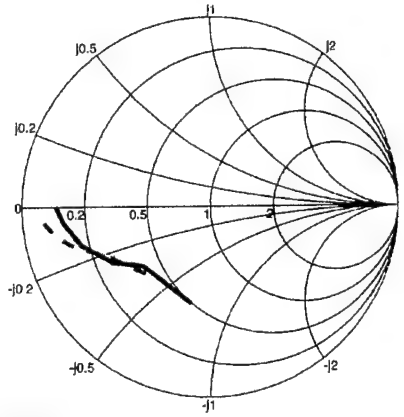


Fig.10(b) Measured and Modeled P_{in}-P_{out} Data





SIMULATED

MODELED

MEASURED

Fig. 10(c) S11 Data

Fig. 10(d) S22 Data

the gate oxide (gate is at ground during breakdown simulations). This leads to a large electric field in the oxide region, and a correspondingly large field in the silicon substrate underneath the gate. Depletion charge is required in silicon to support this voltage across the oxide. This charge can be generated in a very shallow region for the heavily doped drain region; however, the lightly doped substrate has to be depleted much more significantly to support this voltage. This corresponds to a large vertical electric field. These field lines terminate in the poly. So, breakdown takes place by impact generation in the substrate region just beyond the heavily doped n^+ drain region.

This causes the breakdown voltage to remain constant for a given oxide thickness. The additional voltage has to be supported outside the gate region. This is achieved by receding the drain region away from the gate edge and the formation of the LDD region between the gate and drain edges. The doping in the LDD region could be varied to ensure that the breakdown now occurs not at the surface but deeper into the substrate at the edge of the n^+ drain. Ideally, the electric field is expected to be uniformly distributed throughout the LDD region at the time of breakdown. Fig.3 shows the electric field distribution along a horizontal cross section of the device at the time of breakdown. The electric field is shown to be maximum in the LDD region of the device and peaks at the drain and gate edges of the LDD region. The LDD doping affects the parasitics such as C_{oss} and C_{rss}. The doping in the p-body region determines the threshold voltage and also helps to prevent punch through between the drain and source regions.

(ii) Comparison Between Measured and Simulated Results

Extensive 2-D simulations were performed to study DC and RF performances of the device. Results obtained from 2D- device simulations are shown to be in good agreement with the measured results. The device has a V_{BD} of 78 V and a threshold voltage of 2.5 V. Table.2 shows a comparison between the measured and simulated results for the DC performance of the device.

Table 2. Measured and Simulated DC Characteristics

PARAMETER	BIAS CONDITIONS	MEASURED	SIMULATED
V_{BD} (V)	V_{GS} = 0V, I_D = 0.05A	65 (min.)	78
V_{th} (V)	V_{DS} = 0.1 V	2.5	2.5
g_m (mho)	V_{GS} = 5 V, V_{DS} = 10 V	0.8	0.82
R_{on} (Ω)	V_{GS} = 20 V, I_D = 4 A	1	0.95
R_{sp} (mΩ – cm^2)	V_{GS} = 12 V, V_{DS} = 0.1 V	6.2	5.9
I_{Dsat} (A)	V_{GS} = 20V, V_{DS} = 10 V	6.0	6.0
C_{iss} (pF)	V_{GS} = 0 V, V_{DS} = 28 V, F = 1 MHz	30.0	29.2
C_{oss} (pF)	V_{GS} = 0 V, V_{DS} = 28 V, F = 1 MHz	15.0	14.6
C_{rss} (pF)	V_{GS} = 0 V, V_{DS} = 28 V, F = 1 MHz	1.5	1.71

* Width of device = 3.8 cm

As shown in Table 2, a good match is obtained between the measured and simulated results. Fig.4 shows a comparison between the measured and simulated I-V curves for gate voltages from 4 V to 12 V. Figs. 5 to 7 show the comparison of other DC characteristics between the measured and simulated results. The device is operated from a 28 V power supply and a quiescent drain current of 400 mA. The RF operating frequency was 1 GHz.

As discussed earlier, this device is meant to be used in RF power amplifiers for cellular base stations. Hence, the RF characteristics such as power added efficiency, gain, noise figure, intermodulation distortion are the parameters of most concern for this device. The first step towards the RF characterization of this structure is the extraction of S-parameter data. Mixed simulations at the given bias point and operating frequency were performed with the input and output terminals matched to 50 ohms and with and without the package parasitics included. The results show a very good match with the measured data. These parameters are important in determining the RF performance of the device since a proper impedance matching circuitry can be built using the S-parameter data to obtain maximum gain and efficiency.

Because of the nature of applications and also the high power levels involved, this device is expected to generate extensive heat. Hence, it is important to study the performance of this device at different ambient temperatures including the effects of self-heating [16]. Extensive 2D- simulations were performed to determine the DC characteristics of the device from temperatures ranging from -50^0 C to 200^0 C. Fig.7(a) shows the variation in R_{on} and V_{th} with temperature. Fig. 7(b) shows the variation of g_m and I_{Dsat} for this device with temperature. The on-resistance and transconductance of the device are related to the mobility of the carriers. Hence, due to the decrease in the mobility of carriers, the on-resistance is expected to increase and the transconductance is expected to decrease with temperature. An equation has been proposed to predict the variation of on-resistance with temperature for p- and n-channel MOSFETs as follows:

$$R_{on}(T) = R_{on}(25^{o}C)(\frac{T}{300})^{n} \qquad (1)$$

where T is the absolute temperature. The value of n over wide temperature range is about 2.0.

The RF performance of the device was calculated by the use of a circuit model that was developed after careful study and understanding of the device physics. This circuit model was used in SPICE-like simulators [17,18] for performing the desired simulations at RF frequencies. The simulation results obtained from the circuit model are shown to be in close agreement with the actual device measurements for both the DC and high frequency operation as shown in the various plots that follow the description of the model.

(iii) Circuit Model

The circuit model developed for the emulation of the device performance is shown in Fig. 8. This is a simple circuit model consisting of a SPICE Level 1 MOSFET [19,20], a JFET and a diode [21] as the basic elements. This circuit model also includes the parasitic capacitances such as the C_{iss} and C_{rss}. Numerous circuit models for power LDMOSFETs have been reported in the literature [8,12-14]. It is shown in this work that the LDD region offers a non-linear resistance to the current flow, and hence, is equivalent to a JFET in behavior.

Fig. 9 shows the potential across the channel and LDD region for different drain bias voltages. For smaller values of V_{DS}, potential drop along the LDD region is linear, indicating resistive behavior. However, at higher values of V_{DS}, the potential drop becomes highly nonlinear, with more potential

drop towards the gate end of the LDD. This nonlinear distribution of voltage along the LDD indicates that it is not appropriate to model this region as a simple resistor. The pinchoff of the JFET can be seen to occur near the gate edge of the LDD region..

The diode in the circuit is used to model the body diode between the drain and substrate in the device. This is always reverse biased since the substrate is grounded and the variation in the capacitance is actually due to the change in the depletion region of this diode with applied voltage at the drain electrode. The capacitances C_{iss} and C_{rss} are modeled as fixed capacitances measured at quiescent V_{DS}. The body diode in the circuit is used for modeling the variation of C_{oss} with the applied V_{DS}. Thus C_{oss} is modeled with the p-n junction diode capacitance equation :

$$C_{oss} = \frac{C_{JO}}{(1 + \frac{V_{DS}}{V_J})^m} \qquad (2)$$

Table 3 lists the extracted model parameters for the 80V LDMOSFET using the measured data from the experimental device.

Model parameters were extracted for the DMOS large-signal FET model by using the following data :

a) Measured I_D-V_{DS} curves that cover the entire operating range of the device, i.e.
$0 < V_{DS} < 28$ V and V_{GS} for $0 < I_D < I_{Dsat}$

b) Capacitance measurements C_{oss}, C_{iss}, C_{rss} for various values of V_{DS}.

c) S-parameter vs frequency measurements of the DMOSFET biased at the quiescent operating point.

d) RF output versus input power data for the verification of the model.

The following sequence illustrates a systematic procedure for extracting the model parameters.

1. Extract initial parameters for the MOSFET by fitting the MOSFET model to measured I-V data.

a) Set V_{TO} equal to V_{TO} @ I_D = 1 mA from measured I_D-V_{DS} curves.

b) Calculate $K_P = 2(L/W)\frac{I_D}{(V_{GS}-V_{TO})^2}$

from I_D-V_{GS} curves in the linear region. L and W are the gate length and width of the DMOSFET.

c) Calculate $R_T = V_{GS}/I_{DS}$ using the I_D-V_{GS} curves in the linear region of I_{Dmax} curve.

d) Set $R_D = R_S = R_T/2$.

e) Determine LAMBDA to fit the slope of saturated I_D-V_{DS} data for lower I_D curves.

2. Extracting the JFET parameters.

a) Set $V_{TO} = -V_{DS}$ by using the knee at the intersection formed by extending the linear and saturated regions of the I_D-V_{DS} curve with
(V_{GS} = maximum operated V_{GS}) / 2.

b) Find BETA from the value of K_p found for the MOSFET by using the equation
$BETA = K_P(W/L)$

c) Lambda is determined to fit the slope of the I_{Dmax} curve.

3. Final Parameter Extraction.

a) Fit the current level for the curves at lower V_{GS} values by adjusting the values of K_p and lambda. The mid-range I_D-V_{DS} curves can be adjusted by adjusting the values of R_S and R_D so that R_T remains almost constant.

b) Adjust the JFET V_{TO} parameter to adjust the slope as well as level of the upper level I_D-V_{DS} curves.

c) The spacing between the curves for higher V_{GS} can be adjusted by adjusting the value of JFET BETA.

d) The slope of the upper level I_D-V_{DS} curves is adjusted by tweaking the JFET LAMBDA parameter.

e) Adjusting the values of R_S and R_D for the MOSFET help get a good match with the measured data at the end of these steps.

f) The values of C_{iss} and C_{rss} are directly read out from the measured data at the quiescent drain bias.

g) The value of C_{jo} for the diode is set equal to the value of C_{oss} at zero drain bias. The value of C_{oss} at the quiescent drain bias is used to calculate the value of m using equation (2).

h) The values of other parasitics such as the lead inductance, capacitance and resistance for the three electrodes are found through an optimization of the large-signal S-parameters of the DMOSFET at the quiescent bias point.

The above specified parameter extraction methodology was utilized to extract the model parameters for the circuit model of 80 V LDMOSFET. Table 3 shows the extracted model parameters for all the components of the circuit model.

Table 3. Extracted Model Parameters for 80V LDMOSFET

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=2.5, K_p=1.25e-5, LAMBDA=0.15,R_D=0.01, R_S=0.54, L=1.1 μm, W=4 cm
JFET	type=n, V_{TO}=-6.8, BETA=0.95, LAMBDA=0.02
Diode	C_{jo}=45e-12, R_S=0.25,V_j=0.75, m=0.545, V_{BD}=65
C_{iss} (pF)	29.2
C_{rss} (pF)	1.71
R_G (Ω)	0.001
L_G (nH)	0.13
R_D (W)	0.0001
L_D (nH)	1.10
L_S (nH)	0.23

Fig. 10(a) shows the comparison between the measured and modeled results for the I_D-V_{DS} curves. As shown in the figure, the model closely emulates the performance of the experimental device. The S-parameter simulations of this circuit model were performed with the input and output matched to 50 Ω. Figs 10(a) and 10(c) show a good match between the measured, simulated and modeled data for

S_{11} and S_{22}. Impedance matching circuitry was then built for this circuit model to obtain maximum power gain. This circuit was used in harmonic balance simulators to perform large signal AC simulations for calculating the maximum power gain and efficiency. Fig 10(d) shows the measured and simulated data for P_{in}-P_{out} performance of this device. The device gives a maximum gain of 15 dB with a peak input power of 2 W. The drain efficiency of this device has been found to be 55%. Noise figure simulations were performed on this device using the similar matching network as was used for the gain simulations. The noise figure for this device was simulated to be 6.5 dB as compared to the measured noise figure of 5.5 dB. As shown in Fig 10(d) the simulated data from the circuit model for the P_{out} and gain follow the trend of the measured data, although a perfect match has not been obtained. The mismatch is attributed to losses in the matching circuits in a practical amplifier.

Yet another important aspect in the design of LDMOSFETs for power applications is the issue of self-heating [16]. Self-heating could lead to premature breakdown of the device, and could degrade the performance of the device to a considerable extent in case of a large rise in temperature within the device. Two-dimensional non-isothermal simulations were performed using MIXEDMODE [22] to study the self-heating properties of this device. It has been observed that there is no significant rise in the temperature within the device. This is explained by the fact that this is a bulk device, and hence, the heat generated within the device is easily dissipated in the large bulk region [23,24]. No significant changes in the DC or RF parameters have been observed due to self-heating.

C3. Design of 50V LDMOSFETs on Bulk and SOI Substrates

In this work, four new 50V LDMOSFET device structures were studied to understand the behavior of different technologies for RF performance. Two of the devices were built in the conventional bulk silicon. The two devices differ from each other in terms of doping in the epi region. The first device (Str 1) has an n-type epitaxial region and the second bulk structure (Str 2) has an p-type epitaxial region. Str 3 (n-type epi) and Str 4 (p-type epi) were designed using the SOI technology with a 0.3 μm thick buried oxide layer within the device. Extensive DC simulations were performed on all the four devices. Circuit models were extracted for the four devices and validated with the simulated data. RF simulations were performed at 1 GHz using the circuit models. Non-isothermal simulations were performed on the n-type epi devices in bulk and SOI to study the effect of self-heating on the DC and RF performance.

(i) Device Structures

Device structures for simulation of the four devices were created using an advanced process simulator in which the device structure is represented as a 2D- finite element grid. An advanced device simulator which is used to calculate the semiconductor equations at each of the grid points was used to simulate the DC performance. The simulator is also used to solve the heat flow equations to study the local temperature changes within the device due to self-heating. The four device structures are shown in Fig. 11 (a)-(d). The basic topology for the four devices is similar. Figs. 11 (a) and 11 (b) represent the bulk MOSFETs and Figs .11(c) and 11 (d) represent the SOI MOSFETs. Optimum doping levels were arrived at by simulating the breakdown performance of each of the devices using a device simulator. All these devices were designed for breakdown voltage of 50 V. The doping profiles for each of these device structures are shown in Figs. 12(a)-(c). Table 4 gives the feature dimensions for the four devices.

Table 4. Performance comparison of four device structures under study.

Technology	**BULK**		**SOI**	
Parameter	**N-EPI (Str 1)**	**P-EPI (Str2)**	**N-EPI (Str1)**	**P-EPI (Str2)**
t_{ox} (A)	650	650	650	650
t_{epi} (μm)	8	8	8	8
Doping (cm^{-3})				
epi	1.2×10^{15}	1.2×10^{15}	2.0×10^{15}	1.2×10^{15}
p^+ substrate	2.5×10^{18}	2.5×10^{18}	2.5×10^{18}	2.5×10^{18}
p^+ sinker	2.0×10^{19}	2.0×10^{19}	-	-
p base	8.5×10^{17}	8.5×10^{17}	4.0×10^{17}	4.0×10^{17}
n^+ source	2.0×10^{20}	2.0×10^{20}	4.0×10^{20}	4.0×10^{20}
n^+ drain	7.0×10^{19}	7.0×10^{19}	6.7×10^{19}	6.7×10^{19}
n ldd	0.7×10^{17}	0.7×10^{17}	0.3×10^{17}	1.0×10^{17}
Dimension (μm)				
l_s	2.25	2.25	1.0	1.0
l_{so}	2.75	2.75	1.25	1.25
l_g	1.1	1.1	1.2	1.2
l_{ldd}	1.6	1.6	1.2	1.2
l_d	0.75	0.75	0.75	0.75

These devices were designed to operate from a 12 V power supply. Hence, they are required to be able to block up to three to four times the operating voltage that might be seen across the device due to inductive kickback. This is accomplished by the inclusion of the LDD region of the drain extension. In the absence of the LDD region, most of the applied drain voltage appears across the gate oxide (gate is at the ground potential during breakdown simulations). This leads to a large electric field in the oxide region, and a correspondingly large field in the silicon substrate underneath the gate. Depletion charge is required in silicon to support this voltage across the oxide. This charge can be generated in a very shallow region for the heavily doped drain region; however, the lightly doped substrate has to be depleted much more significantly to support this voltage. This corresponds to a large vertical electric field. These field lines terminate in the polysilicon. Hence, breakdown takes place by impact generation in the substrate region just beyond the heavily doped n^+ drain region. This causes the breakdown voltage to remain almost constant for a given oxide thickness. The additional voltage has to be supported outside the gate region. This is achieved by receding the drain region away from the gate edge and the formation of the LDD region between the gate and drain edges. The doping in the LDD region could be varied to

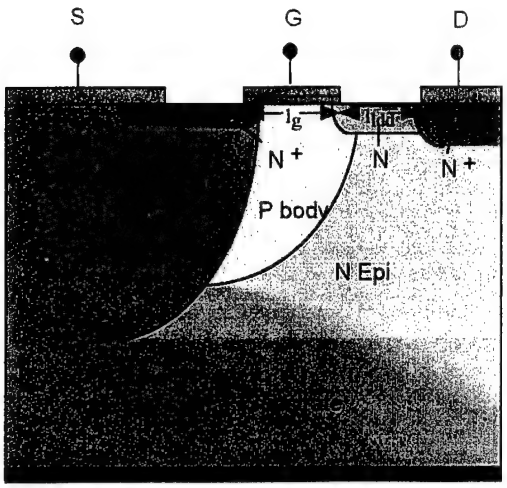


Fig. 11(a) Bulk n-epi device (Str1)

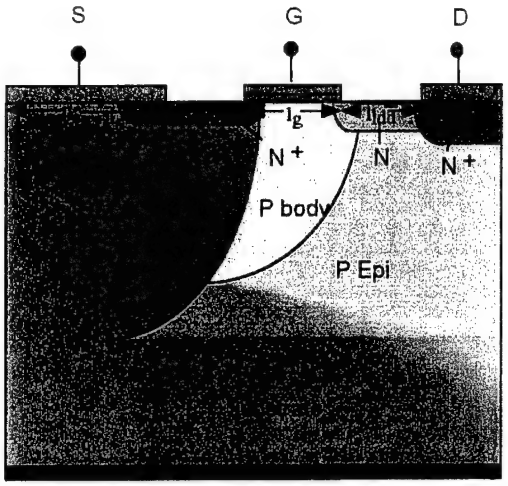


Fig. 11(b) Bulk p-epi device (Str2)

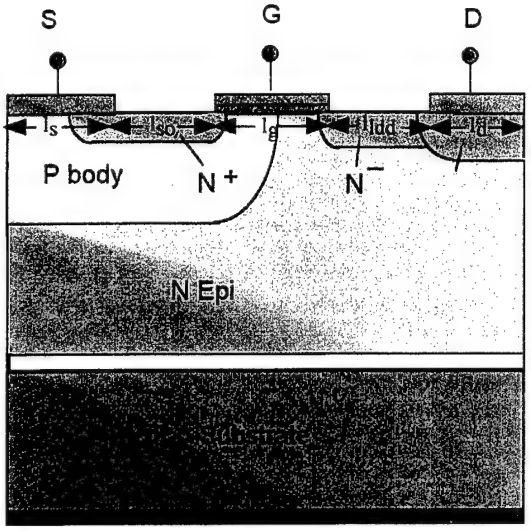


Fig. 11(c) SOI n-epi device (Str3)

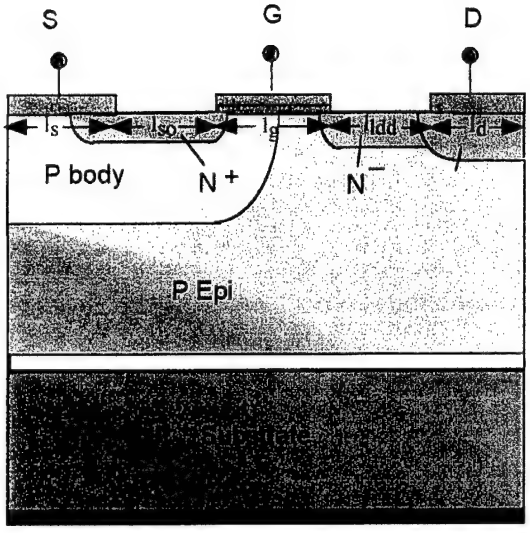


Fig. 11(d) SOI p-epi device (Str4)

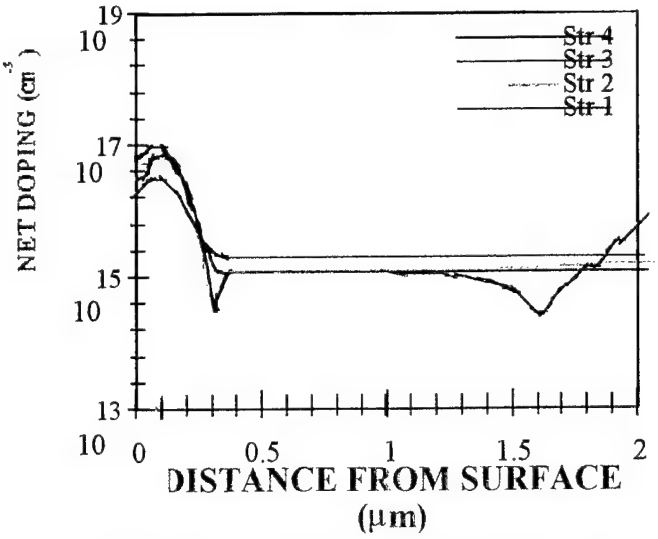


Fig. 12(a) Doping profiles of the LDD region for four devices.

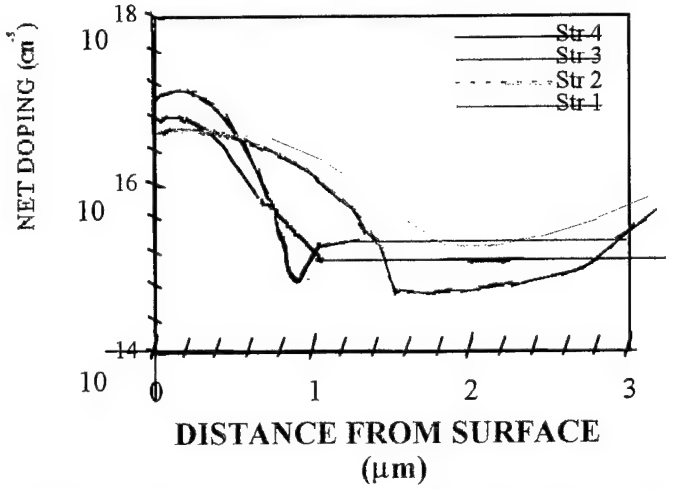


Fig. 12(b) Doping profiles under the gate(in the p-body) for four devices.

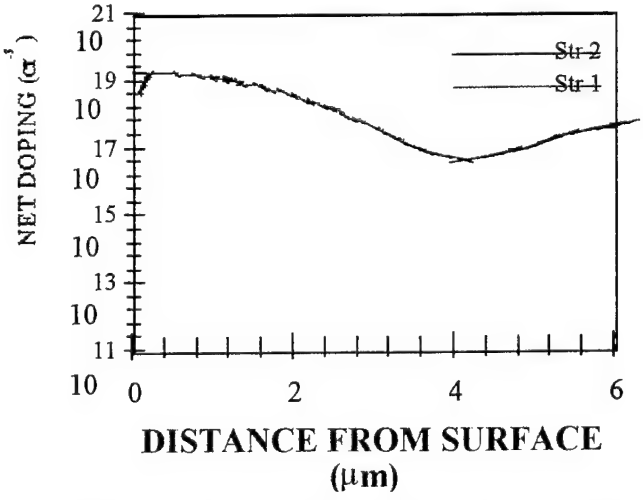


Fig. 12(c) Doping profiles of the sinker region for bulk devices.

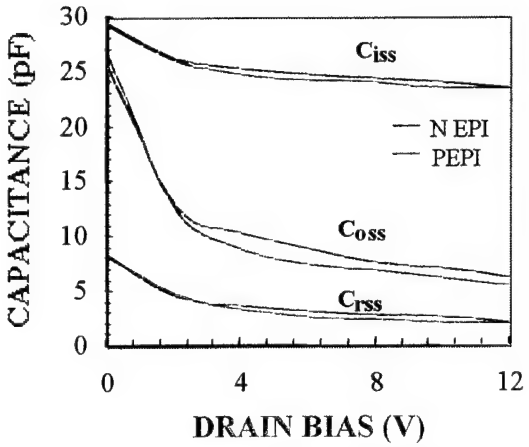


Fig. 13(a) Comparison of C-V plots for bulk devices

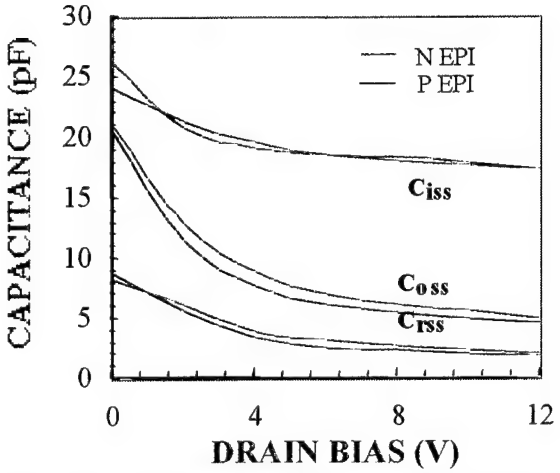


Fig. 13(b) Comparison of C-V plots for SOI devices

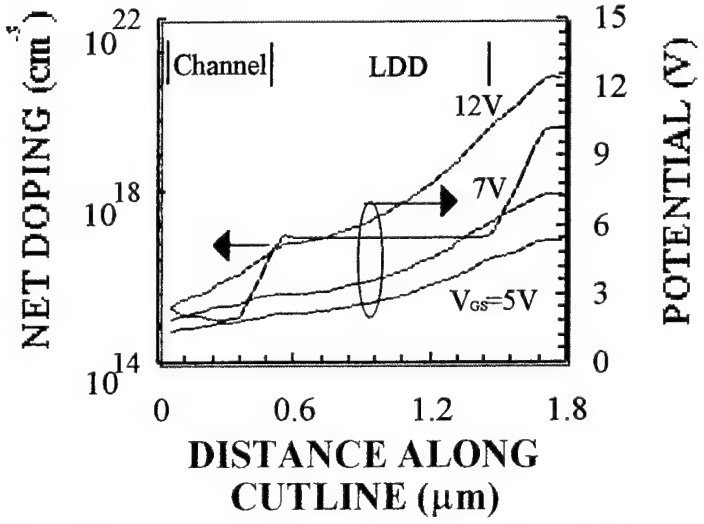


Fig. 14 Variation in potential in LDD and channel with gate bias.

ensure that the breakdown now occurs not at the surface but deeper into the substrate at the edge of the n^+ drain. Ideally, the electric field is expected to be uniformly distributed throughout the LDD region at the time of breakdown.

The p-type body region under the gate forms the channel for the MOSFET. The doping in the p-body region chiefly controls the threshold voltage of the device. From the plot of electric field distribution along a horizontal cross section of the device at the time of breakdown, it can be shown that field is maximum in the LDD region of the device and peaks at the drain and gate edges of the LDD region. The LDD doping affects the parasitic capacitances including C_{oss} and C_{rss}. As shown in Table 4, there is no sinker formation in SOI devices. Hence, due to the absence of sinker region in SOI devices, there is a large reduction in the total length of the device. This causes a large reduction in the specific on-resistance. This could prove to be of great advantage in power amplification applications as it would minimize conduction power loss and reduces self-heating.

(ii) Comparison between DC Performance of the Four Structures

Extensive DC simulations were performed on all the four devices and their performances were compared to predict the optimum device with minimum parasitics and which could give the best RF performance. Table 5 shows the DC performance comparison for the four devices.

Table 5. Simulated DC performance for the four devices

Technology	**BULK**		**SOI**	
Parameter	**(Str 1)**	**Str (2)**	**(Str 3)**	**(Str 4)**
V_{BD} (V)	49.0	49.0	48.5	49.0
V_{th} (V)	1.65	1.64	1.6	1.6
C_{iss} (at zero bias) (pF)	29	29	26.2	24.2
C_{iss} (at V_{DS}=12 V) (pF)	23.5	24.0	17.5	18.0
C_{oss} (at zero bias) (pF)	26.5	24.0	21.0	20.5
C_{oss} (at V_{DS}=12 V) (pF)	5.5	5.0	5.0	4.7
C_{rss} (at zero bias) (pF)	8.2	7.75	8.2	8.75
C_{rss} (at V_{DS}=12 V) (pF)	1.9	1.5	1.6	1.9
R_{on} (V_{GS}=6 V, V_{DS}=0.1V)	1.09	0.96	0.86	0.61
R_{sp} (mΩ-cm^2)	1.06	0.89	0.50	0.46
g_m (at V_{DS}=12V, V_{GS}=6 V)	1.48	1.52	1.75	1.68

* Device width = 4 cm.

Figs. 13(a) and 13(b) show the comparison of the C-V plots for the bulk and SOI devices at V_{DS} of 12 V. As seen from the plots, the parasitic capacitances (C_{oss}, C_{rss}, and C_{iss}) at zero bias for the SOI devices are significantly lower than for the bulk devices. This is an important result to predict the RF performance of these devices. As discussed earlier, the on-resistance of SOI devices is significantly smaller compared to the bulk devices. This leads to lower heat dissipation, and hence, improved power

gain. It is shown in Table 5 that the SOI devices also have a higher transconductance than the bulk devices. This would prove to be a significant parameter for RF applications since this parameter determines the power gain of the transistor.

As discussed earlier, this device is meant to be used in RF applications such as the power amplifiers for cellular base stations. Hence, the RF characteristics such as power added efficiency, gain, noise figure, and intermodulation distortion are the parameters of most concern for this device. The first step towards the RF characterization of this structure is the extraction of S-parameter data. These parameters are important in determining the RF performance of the device since a proper impedance matching circuitry can be built using the S-parameter data to obtain maximum gain and efficiency. It is mandated that a circuit model be developed that would closely emulate the DC and RF performance of these devices. This is required for performing the large signal AC simulations for determining the RF performance. Mixed simulations at the given bias point and operating frequency were performed with the input and output terminals matched to 50 Ω. A simple circuit model was developed through a proper understanding of the device physics as described below.

(iii) Circuit Model

The circuit model developed for the 80V LDMOSFET (illustrated in Fig. 7 in the previous section) was also used to emulate the device performance of all four 50V devices.

Fig. 14 shows the potential across the channel and LDD region for different drain bias voltages. For smaller values of V_{DS}, potential drop along the LDD region is linear, indicating resistive behavior. However, at higher values of V_{DS}, the potential drop becomes highly nonlinear, with more potential drop towards the gate end of the LDD. This nonlinear distribution of voltage along the LDD indicates that it is not appropriate to model this region as a simple resistor. The pinch-off of the JFET can be seen to occur near the gate edge of the LDD region. As in Fig. 7, we have modeled this nonlinear resistor using a JFET.

Table 6(a) Model parameters for Str 1.

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=1.6, K_p=1.5e-5, LAMBDA=0.15,R_D=0.0001, R_S=0.0001, L=0.9 μm, W=4 cm
JFET	type=n, V_{TO}=-4.4, BETA=0.95, LAMBDA=0.03
Diode	V_{BD}=50, C_{jo}=26.5e-12, R_S=0.25,V_j=0.7, m=0.345
C_{iss} (pF)	23.5
C_{rss} (pF)	1.9
R_G (Ω)	0.01
L_G (nH)	0.13
R_D (W)	0.01
L_D (nH)	0.6
L_S (nH)	0.23

Table 6(b) Model parameters for Str 2.

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=1.6, K_p=1.2e-5, LAMBDA=0.18,R_D=0.001, R_S=0.001, L=0.9 μm, W=4 cm
JFET	type=n, V_{TO}=-4.6, BETA=0.85, LAMBDA=0.03
Diode	V_{BD}=50, C_{jo}=29e-12, R_S=0.25,V_j=0.7, m=0.395
C_{iss} (pF)	24.0
C_{rss} (pF)	1.5
R_G (Ω)	0.01
L_G (nH)	0.53
R_D (W)	0.01
L_D (nH)	0.6
L_S (nH)	0.23

Table 6(c) Model parameters for Str 3.

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=1.6, K_p=1.4e-5, LAMBDA=0.17,R_D=0.002, R_S=0.001, L=0.9 μm, W=4 cm
JFET	type=n, V_{TO}=-4.5, BETA=1.2, LAMBDA=0.02
Diode	V_{BD}=50, C_{jo}=21e-12, R_S=0.25,V_j=0.7, m=0.395
C_{iss} (pF)	17.5
C_{rss} (pF)	1.6
R_G (Ω)	0.001
L_G (nH)	0.13
R_D (W)	0.001
L_D (nH)	1.1
L_S (nH)	0.23

The model parameter extraction methodology described in the previous section was utilized to extract the model parameters for the circuit model of 50 V LDMOSFET. Table 6 shows the extracted model parameters for all the components of the circuit model for the four structures. All parameter values are in a range that is physically meaningful.

Table 6(d) Model parameters for Str 4.

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=1.6, K_P=1.6e-5, LAMBDA=0.04,R_D=0.001, R_S=0.0003, L=0.9 μm, W=4 cm
JFET	type=n, V_{TO}=-4.7, BETA=0.95, LAMBDA=0.06
Diode	V_{BD}=50, C_{jo}=20.5e-12, R_S=0.25,V_j=0.7, m=0.345
C_{iss} (pF)	18.0
C_{rss} (pF)	1.9
R_G (Ω)	0.001
L_G (nH)	0.54
R_D (W)	0.001
L_D (nH)	0.6
L_S (nH)	0.23

Both DC and RF simulations were performed using the above circuit models. Figs. 15 (a) - (d) show the comparison between the simulated and modeled I-V curves for the four devices. It is evident from the I-V curves that the SOI devices have larger drain current for a given bias than the bulk devices. A reasonable good match was obtained between the simulated and modeled S-parameter values for the four device models as shown in Figs. 16(a) - 16(d). The S-parameter values were utilized to design the impedance matching networks at the device terminals for performing AC large signal analysis. Figs. 17 (a) and 17 (b) show the comparison of output power and common source power gain for the bulk and SOI devices. The n-epi devices offer more gain than the p-epi devices in the case of both the technologies. Table 7 shows a comparison of the simulated RF parameters for the four devices.

Table 7. Simulated RF performance for the four device structures.

PARAMETER	BIAS CONDITIONS	Str 1	Str 2	Str 3	Str 4
Common Source Power Gain (dB)	P_{in} of 2 W	7.85	9.38	9.52	9.29
Noise Figure (dB)	F = 1 GHz	7.1	6.86	6.91	6.84

Extensive 2D- simulations were performed by including reliable self-heating models for various materials [25]. Non-isothermal simulations were performed to study any variations in the performance of the device due to increase in its internal temperature caused by self-heating. Fig. 18 shows the variation in the on-resistance of the bulk and SOI devices (n-epi) due to self- heating. As evident from the plots, the on-resistance of the SOI device increases more rapidly than for the bulk device. Hence, there is a large variation in the DC characteristics of the SOI device with temperature when compared to the bulk device. Figs. 19 shows the temperature distribution contours from non-isothermal simulations in the SOI n-epi device at V_{GS}= 6V and ambient temperature of 300^{o}C. From these plots it is evident that self-heating causes the maximum rise in temperature in the LDD region. Self-heating is also observed in bulk

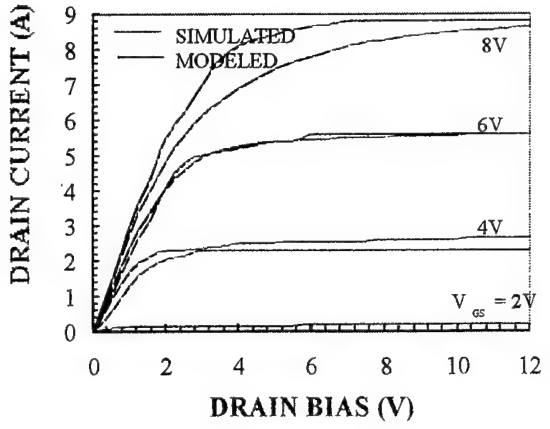


Fig.15(a) I-V curves for Str 1.

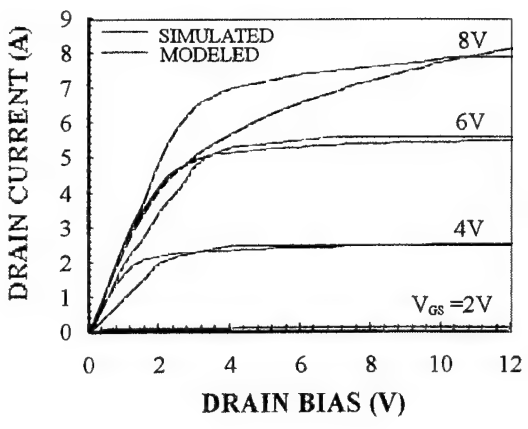


Fig.15(b) I-V curves for Str 2.

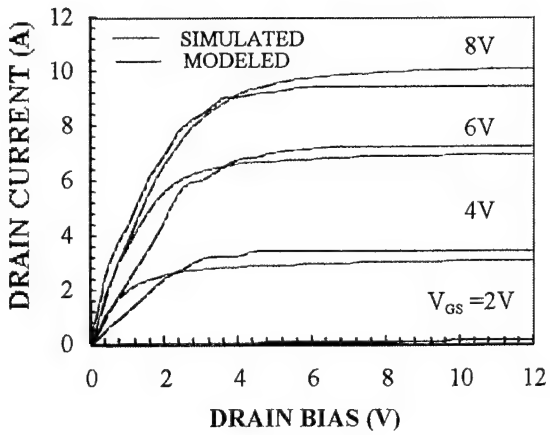


Fig.15(c) I-V curves for Str 3.

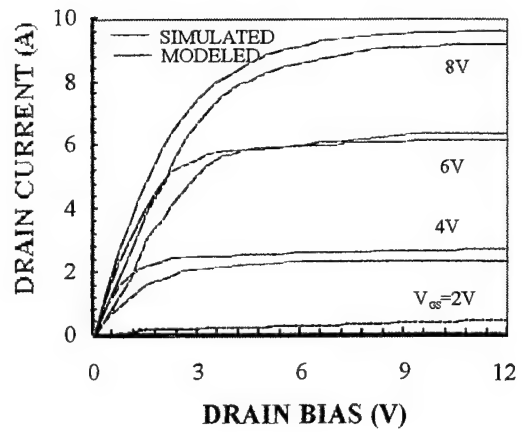


Fig.15(d) I-V curves for Str 4.

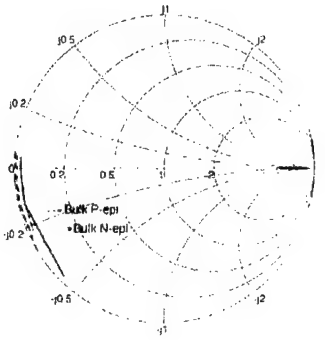


Fig.16(a) S11 data for bulk devices

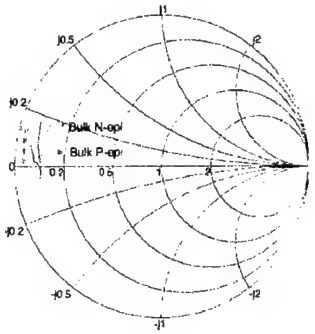


Fig.16(b) S22 data for bulk devices

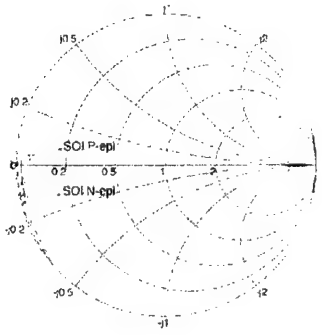


Fig.16(c) S11 data for SOI devices

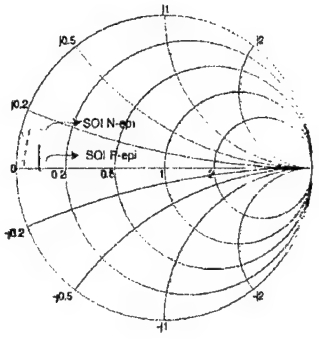


Fig.16(d) S22 data for SOI devices

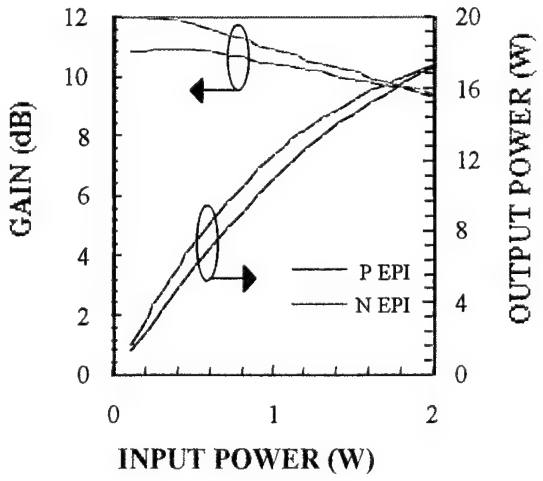


Fig.17(a) P_{in}-P_{out} data for bulk devices

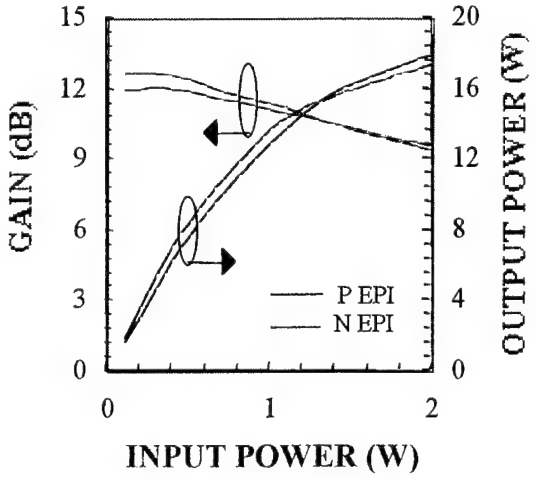


Fig.17(b) P_{in}-P_{out} data for SOI devices

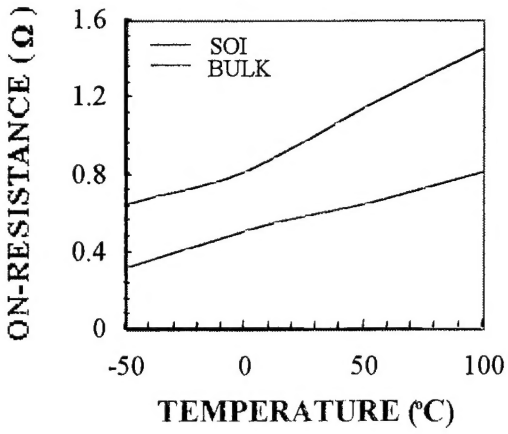


Fig.18 variation in on-resistance with temperature

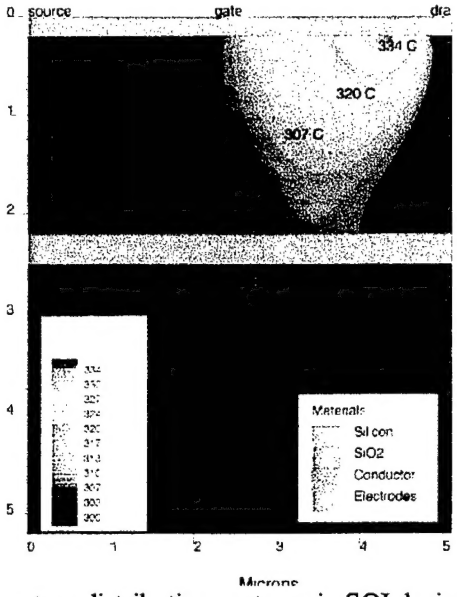


Fig.19 Temperature distribution contours in SOI device die to self heating

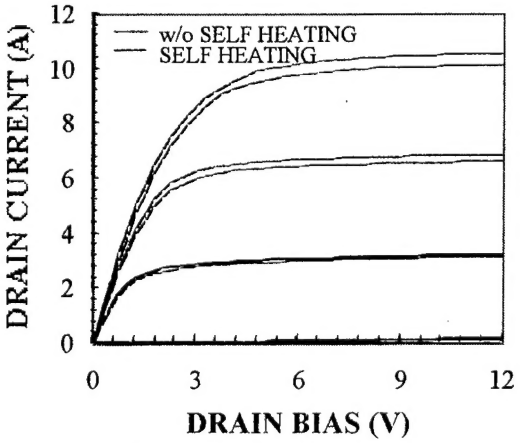


Fig.20 variation in I-V curves of SOI device due to self heating effect.

devices. However, in the bulk device, the higher temperature is concentrated only in a very small region around the LDD. However, in the case of the SOI device, there is an increase in temperature over a major portion of the active area because of the difficulty for heat diffusion due to the existence of an insulating oxide layers. This issue needs to be further studied in Phase II since it could lead

Table 8(a). Model parameters for Str 1 at 75 ^{o}C.

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=1.3, K_p=1.3e-5, LAMBDA=0.15,R_D=0.0001, R_S=0.0001, L=0.9 μm, W=4 cm
JFET	type=n, V_{TO}=-4.6, BETA=0.95, LAMBDA=0.04
Diode	V_{BD}=50, C_{jo}=26.5e-12, R_S=0.25,V_j=0.7, m=0.345
C_{iss} (pF)	23.5
C_{rss} (pF)	1.9
R_G (Ω)	0.01
L_G (nH)	0.13
R_D (W)	0.01
L_D (nH)	0.6
L_S (nH)	0.23

Table 8(b) Model parameters for Str 1 at 125 ^{o}C.

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=1.15, K_p=1.2e-5, LAMBDA=0.07,R_D=0.001, R_S=0.001, L=0.9 μm,W=4 cm
JFET	type=n, V_{TO}=-4.9, BETA=0.85, LAMBDA=0.03
Diode	V_{BD}=50, C_{jo}=29e-12, R_S=0.25,V_j=0.7, m=0.395
C_{iss} (pF)	24.0
C_{rss} (pF)	1.5
R_G (Ω)	0.01
L_G (nH)	0.53
R_D (W)	0.01
L_D (nH)	0.6
L_S (nH)	0.23

to premature device breakdown and electromigration. Fig. 20 shows a comparison between the simulated I-V curves for the n-epi SOI device obtained from isothermal and non-isothermal simulations. It is evident from these results that there is an increase in the on-resistance and a reduction in the drain saturation current due to self-heating. No change in capacitances were simulated due to increase in the lattice temperature within the device.

Table 8(c) Model parameters for Str 3 at 75 ^{o}C.

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=1.4, K_p=1.2e-5, LAMBDA=0.10,R_D=0.006, R_S=0.005, L=0.9 μm, W=4 cm
JFET	type=n, V_{TO}=-4.65, BETA=1.2, LAMBDA=0.02
Diode	V_{BD}=50, C_{jo}=21e-12, R_S=0.25,V_j=0.7, m=0.395
C_{iss} (pF)	17.5
C_{rss} (pF)	1.6
R_G (Ω)	0.001
L_G (nH)	0.13
R_D (W)	0.001
L_D (nH)	1.1
L_S (nH)	0.23

Table 8(d) Model parameters for Str 3 at 125 ^{o}C.

Component	Value
MOSFET (level - 1)	type=n, V_{TO}=1.25, K_p=1.2e-5, LAMBDA=0.02,R_D=0.01, R_S=0.003, L=0.9 μm, W=4 cm
JFET	type=n, V_{TO}=-4.9, BETA=0.95, LAMBDA=0.09
Diode	V_{BD}=50, C_{jo}=20.5e-12, R_S=0.25,V_j=0.7, m=0.345
C_{iss} (pF)	18.0
C_{rss} (pF)	1.9
R_G (Ω)	0.001
L_G (nH)	0.54
R_D (W)	0.001
L_D (nH)	0.6
L_S (nH)	0.23

Because of the nature of applications, it is important to consider the high-temperature performance of these devices. The DC simulations were performed to study the behavior of the n-epi devices at various ambient temperatures. Circuit models were extracted from the simulated data for the emulation of the device performance at 75^{o}C and 125^{o}C. There is a sharp increase in the on-resistance of the devices at higher ambient temperatures. This is caused by the inverse dependence of the on-resistance of the LDMOSFET on mobility. The mobility of the carriers decreases with increase in the temperature. With a similar reasoning, the transconductance also decreases with temperature. Circuit models for bulk and SOI n-epi devices at higher temperatures are given in Table 8.

C4 Conclusions

In conclusion, four 50V LDMOSFET device structures were designed and optimized for RF performance and a comparative study has been made to determine the optimum technology for Phase II development and commercialization. Lower parasitics and on-resistance make SOI devices better suited for RF applications than their bulk counterparts. Devices built on n-type epitaxial layer offer better RF gain than the p-epi devices. Non-isothermal simulations made on the n-epi SOI device suggest that for the feature sizes under consideration (about 1 μm), self heating, which is a prime matter of concern in the wide spread use of SOI technology, does not deteriorate the DC performance of the device significantly. However, more definitive numerical simulations including the package thermal resistance and improved second-order physics models need to be performed for a critical evaluation. These results are very encouraging and provide impetus for further development and commercialization of SOI RF LDMOSFETs in Phase II.